
The custom integrated circuits

Most of the circuitry that controls memory and I/O addressing in the Apple IIe is in three custom integrated circuits called the Management Unit (MMU), the Input/Output Unit (IOU), and the Programmed Array Logic device (PAL). The soft switches used for controlling the various I/O and addressing modes of the Apple IIe are addressable flags inside the MMU and the IOU. The functions of these two devices are not as independent as their names suggest; working together, they generate all of the addressing signals. For example, the MMU generates the address signals for the CPU, while the IOU generates similar address signals for the video display.

The Memory Management Unit

The circuitry inside the Memory Management Unit (MMU) implements these soft switches, which are described in the indicated chapters in this manual:

- ☐ Page 2 display (PAGE2): Chapter 2
- ☐ high-resolution mode (HIRES): Chapter 2
- ☐ store to 80-column card (80STORE): Chapter 2
- ☐ select bank 2: Chapter 4
- ☐ enable bank-switched RAM: Chapter 4
- ☐ read auxiliary memory (RAMRD): Chapter 4
- ☐ write auxiliary memory (RAMWRT): Chapter 4
- ☐ auxiliary stack and zero page (ALTZP): Chapter 4
- ☐ slot ROM for connector #3 (SLOT3ROM): Chapter 6
- ☐ slot ROM in I/O space (SLOTXROM): Chapter 6

The 64K dynamic RAMs used in the Apple IIe use a multiplexed address, as described later in this chapter in the section "Dynamic-RAM Timing." The MMU generates this multiplexed address for memory reading and writing by the 65C02 CPU. The pinouts and signal descriptions of the MMU are shown in Figure 7-2 and Table 7-6.